



ELECS INDUSTRY CO., LTD.

# HARDWARE CORRELATOR

High Speed and Broadband  
Signal Analysis Solution

**K-3(NICT)**  
XF, 8Msps, 128lag, 1BL First  
operational correlator in Japan



**NAOCO(NAOJ)**  
XF, 128Msps 512lag, 1BL  
Compact portable correlator



**NRFD(JAXA)**  
XF, 256Msps, 4096lag, 1BL  
Fringe detector for VSOP

**UWBC(NAOJ)**  
XF, 4Gsps, 512lag, 21BL Ultra wide band  
correlator for Nobeyama Millimeter Array



2014

1983



**OCTAD-C(Ibaraki Univ.)**  
FX, 4Gsps, 32kch, 6BL Real  
time correlator with built in  
ADC for Takahagi telescope



**VCS(KASI)**  
FX, 4Gsps, 256kch,  
120BL Central correlator  
for KVN and VERA



**BEARS(NAOJ)**  
XF, 1Gsps, 1024lag, 25IF  
25-beam wide band auto  
correlator for Nobeyama  
45m telescope



**e-VLBI(NAOJ)**  
XF/FX, 1Gsps, 16kch, 3BL Real time correlator  
for optically-linked VLBI(OCTAVE)

**WHSF(NAOJ)**  
F-FX, 4Gsps, 16kch, 2IF F-FX wide band  
auto correlator for ASTE telescope

## Technical Advantages

- As a leading company of radio astronomy, Elecs has been developing Hardware Correlator over 30 years.
- Offer perfect technical supports for Proposal/Design/Manufacture/Test/Delivery/Operation.
- Provide up to 20 years long term maintenance contract (request basis).



## Worldwide Installations

Korea

Japan

1983 Ibaraki Kashima

1992 Iwate Mizusawa

1993 Nagano Usuda

1998 Nagano Nobeyama

2001 Tokyo Mitaka

2005 Chile Atacama

2009 Korea Daejeon

2014 Ibaraki Takahagi

## Key-Technology

Architecture	XF, FX
Data Input	10/40/100GbE, VDIF, VTP, VSI-H
Bit Weight	Weight table customization
Delay Compensation	Using a volume of DDR3/4 memory for correction of the delay from the Earth's center
Fringe Rotation	Time domain method, Frequency domain method
FFT	Original IP and XILINX IP
Fractional Delay( $\Delta W$ )	Apply to every FFT segment
Correlation	Special structure for huge baselines
Data Output	UDP/IP, TCP/IP
Parameter Calculation	Built in hard parameter generation, and delay prediction from star/station positions

Chile

## Total System

SAMPLER	VDIF output sampler with digital signal processing
VDIF VSI-H MC	VDIF $\leftrightarrow$ VSI-H Media Converter
DATA RECORDER	VDIF storage with removable storage module
Web GUI SOFTWARE	Equipment control/Data analysis software

## Design Process

Specification	Best suited specification for the purpose of observation
Processing Logic	Verification of characteristic and error by simulation(MATLAB) Finds the best suited operation word length
FPGA	Altera, Xilinx High-End FPGA VHDL, SIMULINK assured implementation
Circuit Board	High Speed I/O(Max25Gbps) simulation Power integrity simulation Flexible board design
Firm ware	RTOS, Linux
Test	Cross checking with simulation Performance check by real observation data

## Correlation System(example) -VCS for KJCC-

Number of stations	16 station
Number of input	512MHz(1024Msps-2bit)x 4 IF
Number of correlation	120(cross)+16(auto)
Processing speed	4Gsps
Architecture	FX
FFT points, word length	256k-points, 20bits-complex

